CLAIMS

1. An auto power saving device for multi-channel transceiver comprising: at least one tier and five levels, the five levels comprising: an input level for each tier having at least one input and producing a time delayed binary signal, a NAND gate level having one NAND gate for each tier, each NAND gate receiving a signal from its respective input and from the output of an upper neighboring NAND gate if such NAND gate exists and from the output of a lower neighboring NAND gate if such NAND gate exists, an inverter level comprising one inverter per tier receiving and inverting said signal from its respective NAND gate, and a NOR gate level comprising one NOR gate that receives all inputs from all inverters on all tiers, and an Output Level producing an output signal.
2. The device of claim 1, wherein all NAND gates have three inputs, wherein the output signal of the lowest NAND gate is introduced into the input of the highest signal.
3. The device of claim 1, wherein an extra input is introduced into the input of the first tier NAND gate so that the first tier input shares its NAND gate with the extra input.
4. The device of claim 1, wherein a plurality of extra inputs is introduced into open NAND gate inputs, wherein the NAND gates have more than 3 inputs.
5. The device of claim 1, wherein a high signal input in the input level indicates an activity input status, and a high signal output indicates a power off command.
6. The device of claim 1, wherein a low signal input in the input level indicates a no activity input status, and a low signal output indicates a non-power off command.
7. An auto power signal device for multi-channel transceiver power state processing comprising: an input level receiving a plurality of time delayed binary signals, a NAND gate level having a plurality of NAND gates receiving a signal from the input level, each NAND gate output introduced into the input of another NAND gate, an inverter level having a plurality of inverters receiving and inverting said signal from

the NAND gate level, a NOR gate level having a NOR gate receiving all inputs from all inverters, and an Output Level outputting an output signal.

8. The device of claim 7, wherein all NAND gates have three inputs, wherein the output signal of the lowest NAND gate is introduced into the input of the highest signal.

9. The device of claim 7, wherein an extra input is introduced into the input of the first tier NAND gate so that the first tier input shares its NAND gate with the extra input.

10. The device of claim 7, wherein a plurality of extra inputs is introduced into open NAND gate inputs, wherein the NAND gates have more than 3 inputs.

11. The device of claim 7, wherein a high signal input in the input level indicates an activity input status, and a high signal output indicates a power off command.

12. The device of claim 7, wherein a low signal input in the input level indicates a no activity status, and a low signal output indicates a non-power off command.

13. An auto power saving method for multi-channel transceiver comprising the steps of: providing at least one tier; providing five levels comprising: providing an input level for each tier having at least one input and producing a time delayed binary signal, providing a NAND gate level having one NAND gate for each tier, each NAND gate receiving a signal from its respective input and from the output of an upper neighboring NAND gate if such NAND gate exists and from the output of a lower neighboring NAND gate if such NAND gate exists, providing an inverter level comprising one inverter per tier receiving and inverting said signal from its respective NAND gate, and providing a NOR gate level comprising one NOR gate that receives all inputs from all inverters on all tiers, and providing an output level and producing an output signal.

14. The method of claim 13, further comprising the step of using all three input NAND gates and introducing the output signal of the lowest NAND gate into the input of the highest signal.

15. The method of claim 13, further comprising the step of introducing an extra input into the input of the first tier NAND gate so that the first tier input shares its NAND gate with the extra input.

16. The method of claim 13, further comprising the step of introducing extra inputs into open NAND gate inputs, wherein the NAND gates have more than 3 inputs.

17. The method of claim 13, further comprising the step of indicating an activity status with a high signal input in the input level, and indicating a power off command with high signal output.

18. The method of claim 13, further comprising the step of indicating a no activity status with a low signal input in the input level, and indicating a non power off command with low signal output.